In the Abstract:

Please amend the Abstract as follows:

A memory device includes a data line and a variable delay precharge circuit that receives a column bank address signal and a write enable signal and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of the write enable signal. For example, the variable delay precharge circuit may include a precharge circuit operative to precharge the data line responsive to a precharge control signal, and a variable delay precharge control signal generator circuit that receives the column bank address signal and the write enable signal and that delays the precharge control signal with respect to the column bank address signal responsive to the write enable signal. ~~The variable delay precharge circuit may precharge the data line after a first predetermined time period following assertion of the column bank address signal when the write enable signal indicates a read operation, and may precharge the data line after a second predetermined time period following assertion of the column bank address signal when the write enable signal indicates a write operation. The second time period may be shorter than the first time period.~~